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10/608,187	06/30/2003	Heume II Baek	054358-5097	8785

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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/608,187	BAEK ET AL.	
	Examiner	Art Unit	
	JEFF PIZIALI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2009 and 27 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7-9 and 12-14* is/are pending in the application.

4a) Of the above claim(s) *4,5,7-9 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. *Claim 1* is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 1 recites the limitation "***the data line***" (*line 4*). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether the above limitation is intended to be identical to, common to, or distinct from "***a plurality of data lines***" (*line 4*) and/or "***one data line***" (*line 6*).

4. Claim 1 recites the limitation "***the thin film transistor***" (*line 12*). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether the above limitation is intended to be identical to, common to, or distinct from "***a plurality of thin film transistors***" (*line 3*).

5. Claim 1 recites the limitation "***the gate voltage***" (*line 24*). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether the above limitation is intended to be identical to, common to, or distinct from "***a plurality of gate voltages***" (*line 8*) and/or "***each of the gate voltages***" (*line 11*).

6. Claim 1 recites the limitation "***the scan pulse***" (*line 30*). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether the above limitation is intended to be identical to, common to, or distinct from "***a plurality of scan pulses***" (*line 25*) and/or "***each of the scan pulses***" (*line 26*).

7. The claim is rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejection(s) over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claim, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. *Claim 1* is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Hasegawa et al (US 6,335,717 B1)*** in view of ***Saishu et al (US 5,949,391 A)***.

Regarding Claim 1, ***Hasegawa*** discloses a method of driving a ferroelectric liquid crystal display device [*e.g., Fig. 2*] including

a liquid crystal panel [*e.g., Fig. 2: 10*] having

a plurality of data lines [*e.g., Fig. 3C: 23*],

a plurality of gate lines [*e.g., Fig. 3C: at least two gate lines 24*]:

a plurality of thin film transistors [*e.g., Fig. 3C: 12*] arranged in a zigzag configuration along a direction of the data line [*e.g., Fig. 3A: wherein along the vertical direction of the second left-most column data line, TFT(row=1,column=1) is in a "zigzag configuration" relative to TFT(2,2); TFT(1,3); TFT(2,4); etc.*] and

a ferroelectric liquid crystal material [*e.g., Fig. 3B: 21*] (*e.g., see Column 7, Line 15 - Column 9, Line 4*), wherein

a plurality of pixels [*e.g., Fig. 3A: 3C*] are defined by crossing the gate lines and the data lines, and

one data line is arranged between adjacent pixels [*e.g., see Fig. 3A*],

the method comprising:

supplying a plurality of gate voltages [*e.g., Fig. 4F: Vg*] to the plurality of gate lines during an electric field alignment [*e.g., alignment treatment*] of the ferroelectric liquid crystal material, wherein

each of the gate voltages is set at a level higher than a threshold voltage of the thin film transistor,

the gate voltages are generated in a range of from ten to four-hundred times during the electric field alignment [*e.g., Vg operating at 60Hz for 1 second results in Vgh being supplied 60 times*], and

each gate voltage is simultaneously supplied to the plurality of gate lines (*e.g., Fig. 5: "2 lines at a time scanning pulse"*);

supplying a first data voltage [*e.g., Fig. 5: Vsig*] for the electric field alignment to the plurality of data lines in response to each gate voltage, wherein

a polarity [*e.g., Fig. 5: +2.5 volts, -2.5 volts*] of the first data voltage is inverted every time when [*e.g., Fig. 5: Vsig also operates at 60Hz at Sample No. 6*] the gate voltage is supplied (*see the entire document, including Column 10, Line 46 - Column 11, Line 41*).

Hasegawa discloses the gate voltage can be simultaneously supplied to all of the gate lines in the entire display panel (*e.g., see Column 10, Line 8*); and further

Hasegawa discloses the gate voltage can be simultaneously supplied to any number of gate lines [*e.g., half of the whole display; two gate lines; 10+ gate lines, etc.*] desired (*e.g., see Column 22, Line 1-6*).

Hasegawa discloses an electric field alignment method for a ferroelectric liquid crystal display; but does not appear to discuss a "*normal*" image driving method for the display.

Saishu discloses a method of driving a ferroelectric liquid crystal display device [*e.g., Fig. 1A*] including

a liquid crystal panel [*e.g., Fig. 1A: 10*] having

a plurality of data lines [*e.g., Fig. 2: 18, 20*],

a plurality of gate lines [*e.g., Fig. 2: 16, 17*]:

a plurality of thin film transistors [*e.g., Fig. 2: 12a, 12b*] arranged in a zigzag configuration along a direction of the data line (*e.g., see Column 7, Lines 14-65*) and

a ferroelectric liquid crystal material (*e.g., see Column 10, Lines 50-65*), wherein

a plurality of pixels [*e.g., Fig. 2: 11*] are defined by crossing the gate lines and the data lines, and

one data line is arranged between adjacent pixels [*e.g., Fig. 2: wherein the middle data line 18 is arranged between the left column pixels and the right column of pixels*],

the method comprising:

sequentially supplying a plurality of scan pulses [*e.g., Fig. 3: SAi-1; SBi-1; SAi; SBi; SAi+1*] to the plurality of gate lines [*e.g., Fig. 2: SAi-1; SBi-1; SAi; SBi; SAi+1*] during normal driving for image display, wherein

each of the scan pulses is generated for one horizontal period (*e.g., 1H time is 32 microseconds*) and is supplied to one of the plurality of gate lines; and

supplying a second data voltage [*e.g., Fig. 3: S*] for the image display to the plurality of data lines in response to each scan pulse, wherein

a polarity of the second data voltage is inverted every (*e.g., frame*) time when the scan pulse is supplied (*see the entire document, including Column 7, Line 50 - Column 8, Line 67*).

Hasegawa and ***Saishu*** are analogous art, because they are from the shared inventive field of driving ferroelectric liquid crystal display devices.

Therefore, it would have been obvious to use ***Saishu's*** "*normal*" image driving method and zigzag configuration with ***Hasegawa's*** "*electric field alignment*" method,

so as to provide improved displayed images with high display contrast, no afterimage due to residual hysteresis, and no image sticking and flicker due to ununiform distribution of impurities (***Saishu**: Column 2, Lines 50-58*), and

so as to easily restore the liquid crystal alignment, even if the driving circuit and the like are mounted, and can always display an image of high contrast and good quality (***Hasegawa**: Column 3, Lines 33-37*).

Response to Arguments

11. Applicant's arguments filed on *27 July 2009* have been fully considered but they are not persuasive.

The Applicant contends, "*First, in the claimed invention, a plurality of gate voltages and a first data voltage are supplied during an electric field alignment, and then a plurality of scan pulses and a second data voltage are supplied during a normal driving.* ***Hasegawa** and **Saishu**, whether taken individually or in combination, fail to disclose at least this feature of the claimed invention*" (see Page 10 of the Response filed on *27 July 2009*). However, the examiner respectfully disagrees.

Hasegawa discloses an electric field alignment method for a ferroelectric liquid crystal display (*wherein a plurality of gate voltages [e.g., Fig. 4F: Vg] and a first data voltage [e.g., Fig. 5: Vsig] are supplied during an electric field alignment*); but does not appear to discuss a "*normal*" image driving method for the display.

However, ***Saishu*** discloses a plurality of scan pulses [*e.g., Fig. 3: SAi-1; SBi-1; SAi; SBi; SAi+1*] and a second data voltage [*e.g., Fig. 3: S*] are supplied during a normal driving.

The Applicant contends, "*Second, in the claimed invention, one data line is arranged between adjacent pixels. In **Saishu**, two signal lines 18 and 20 are arranged between adjacent pixels. Thus, **Saishu** fails to disclose at least this feature of the claimed invention*" (see Page 10 of the Response filed on *27 July 2009*). However, the examiner respectfully disagrees.

If "*In **Saishu**, two signal lines 18 and 20 are arranged between adjacent pixels*" (as the Applicant alleges), then *one data line must inherently be arranged between adjacent pixels.*

The Applicant contends, "*Third, in the claimed invention, each gate voltage is simultaneously supplied to the plurality of gate lines. On the contrary, in **Hasegawa**, each signal Vg is supplied to two scanning lines 24 or scanning lines 24 contained in each group. In **Saishu**, each scan signal is supplied to one signal line. Thus, **Hasegawa** and **Saishu**, whether taken individually or in combination, fail to disclose at least each gate voltage simultaneously supplied to all of the gate lines of the claimed invention*" (see Page 11 of the Response filed on *27 July 2009*). However, the examiner respectfully disagrees.

Hasegawa discloses the gate voltage can be simultaneously supplied to all of the gate lines [*e.g., Fig. 3C: gate lines 24*] in the entire display panel (*e.g., see Column 10, Line 8*); and further

Hasegawa discloses the gate voltage can be simultaneously supplied to any number of gate lines [*e.g., be it half of the whole display; or only two gate lines; or 10+ gate lines, etc.*] desired (*e.g., see Column 22, Line 1-6*).

Hasegawa's gate lines [*e.g., the entire display's gate lines; or half of the display's gate lines; or just two gate lines; or 10+ gate lines,*] reads on the instantly claimed "*a plurality of gate lines*."

Applicant's arguments with respect to *claim 1* has been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
6 February 2010